"Handbook of Multilevel Metallization for Integrated Circuits" by Wilson et al. Applicants respectfully request reconsideration and withdrawal of those rejections.

A. Independent Claim 1

Independent Claim 1 recites a semiconductor structure comprising first and second semiconductor regions and a titanium layer characterized by a line width no greater than 0.3μm. Claim 1 also recites a relationship between the thicknesses of the second semiconductor region and the titanium layer that allows the second semiconductor region and the titanium layer, when reacted together, to form titanium disilicide that anneals to a phase with a sheet resistance less than 3 ohms/square. In the Office Action, it was asserted that Hu et al. teaches the recited line width (no greater than 0.3μm) and that Figure 16 of Wilson et al. teaches the recited sheet resistance (less than 3 ohms/square). It was also asserted that obtaining titanium disilicide with both the recited line width and the recited sheet resistance is not dependent on the thickness relationship recited in independent Claim 1. Applicants respectfully disagree.

There is no teaching in Hu et al. or Wilson et al. that the sheet resistance shown in Figure 16 of Wilson et al. can be achieved with the fine line width disclosed in Hu et al. (0.25μm). As explained in Applicants' background section, as line width decreases, it becomes more difficult to transform the C49 $TiSi_2$ films on top of the narrow lines into a C54 phase by thermal annealing due to a lack of nuclei. This can result in $TiSi_2$ films in narrow lines that are still in the high-resistivity C49 phase, or a combination of C49 and C54 phases, even after high temperature annealing, with attendant higher resistivity than if the film were completely in the C54 phase. Because of this "fine line effect," the sheet resistance of the structure disclosed in Hu et al. would be greater than the recited sheet resistance, even if the titanium thickness were chosen according to Figure 16 in Wilson et al.

Applicants discovered a way in which the recited sheet resistance can be achieved with the recited line width. Applicants have found that the thickness of the second semiconductor region (t1) and the thickness of the titanium layer (t2) play an important role in determining completeness of conversion of the titanium disilicide wires from the C49 phase to the C54 phase. Specifically, when $t1 > 1.2\ t2$ and when t1/t2 is sufficiently large, the titanium layer and the second semiconductor region can form titanium disilicide that anneals to a phase with a sheet resistance less than 3 ohms/square. The proposed combination does not disclose these thicknesses and, therefore, does not disclose the semiconductor structure recited in independent Claim 1.

Applicants additionally note that the passage in Hu et al. cited in the Office Action for purportedly teaching the recited dopant concentrations of the first and second semiconductor regions is a patent claim that merely mentions the phrase "a C-54 titanium silicide layer." There is no disclosure in that cited passage of the dopant concentrations recited in independent Claim 1 of the first and second semiconductor regions. Further, in the Office Action, the Examiner noted the similarities between the results shown in Figure 16 of Wilson et al. and those shown in Figure 5 of Applicants' specification. In response, Applicants state that the results in Figure 16 of Wilson et al. are not for the same line width as that shown in Figure 5 in Applicants' specification. Finally, Applicants note that the proposed combination fails to disclose another element recited in independent Claim 1: t1/t2 is sufficiently small such that, when the titanium layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide is in ohmic contact with the first semiconductor region.

In summary, because the proposed combination of Hu et al. and Wilson et al. does not yield the invention recited in independent Claim 1, the rejections of independent Claim 1 and its dependent claims should be withdrawn.

B. Independent Claim 7

Independent Claim 7 recites a semiconductor structure comprising a set of titanium silicide conductors. Independent Claim 7 also recites that each conductor is characterized by a width no greater than 0.3μm and that at least 90% of the conductors are characterized by a sheet resistance less than 3 ohms/square. Independent Claim 7 was rejected in view of the proposed combination of Hu et al. and Wilson et al. Like the rejection against independent Claim 1, this rejection is based on a false premise — that the sheet resistance shown in Figure 16 of Wilson et al. is a characteristic of the 0.25μm titanium silicide in Hu et al. As discussed above, the fine line effect prevents the structure disclosed in Hu et al. from having the sheet resistance shown in Figure 16 of Wilson et al. Because the proposed combination of Hu et al. and Wilson et al. fails to disclose the recited conductor width and sheet resistance, the rejections of independent Claim 7 and its dependent claims should be withdrawn.

IV. The Dependent Claims

While the discussion above focused on deficiencies in the proposed combination with respect to the independent claims, it should be noted that the dependent claims recite further elements not shown in the proposed combination and, therefore, provide additional grounds of patentability. For example, dependent Claim 8 recites that the semiconductor structure comprises a three-dimensional memory array. This feature is not shown or suggested by Hu et al. or Wilson et al. Significantly, the Examiner made no attempt whatsoever in the Office Action to argue that this feature was taught in either of those references.

V. Conclusion

In view of the foregoing amendments and remarks, Applicants submit that this application is in condition for allowance. Reconsideration is respectfully requested. If the Examiner has an questions concerning this Amendment, he is asked to contact the undersigned attorney at (312) 321-4719.

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Respectfully submitted,

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APPENDIX A

Paragraph on page 3, lines 14-25:

Turning now to the drawings, Figure 1 shows a schematic representation of a semiconductor structure 10 that incorporates a preferred embodiment of this invention. The semiconductor structure 10 is a portion of a three-dimensional, field-programmable, write-once memory array of the general type described in co-pending U.S. Patent Application Serial No. 09/928,536 [_____ (Attorney Docket no. 10519/40)], filed on the same day as the present application and hereby incorporated by reference in its entirety. The portion of the memory array shown in Figure 1 includes layers 12, 14, 16 18, and 19 that are patterned with a line width of 0.25 μm. The layer 14 acts as a low-resistivity conductor, and can for example correspond to a word line in a memory array. The layer 19 acts as a dielectric rupture anti-fuse layer, and the layer 18 operates as a diode component. The layers 14, 22 are electrical contacts to the adjacent diode components as well as contacts to the outside world.

APPENDIX B

2. (Amended) The [invention] semiconductor structure of Claim 1 wherein $t1 \geq 2.2t2$.

3. (Amended) The [invention] semiconductor structure of Claim 1 wherein $t1 = 2.3t2, \pm 0.1t2$.

4. (Amended) The [invention] semiconductor structure of Claim 1 wherein t1 is about 600Å and t2 is about 250Å.

5. (Amended) The [invention] semiconductor structure of Claim 1 wherein the dopant concentration of the first semiconductor region is greater than $1x10^{20}/cm^3$.

6. (Amended) The [invention] semiconductor structure of Claim 1 or 5 wherein the first semiconductor region is doped primarily with boron.

8. (Amended) The [invention] semiconductor structure of Claim 1 or 7 wherein the semiconductor structure comprises a 3-D memory array.